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EXAMINER	
SANDOVAL, PATRICK	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/651,113	SARKAR ET AL.	
	Examiner	Art Unit	
	Patrick Sandoval	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12-15,18,19,22-33 and 36-42* is/are rejected.

7)☒ Claim(s) *10, 11, 16, 17, 20, 21, 34, 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date: 9/22/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/651,113 filed on 8/28/2003 has been examined. Claims 1-42 are pending.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. e.g. –Predicting Timing Delay Using Timing Models-- .

Abstract

3. Applicant's abstract is objected to because it includes parenthetical drawing information. Applicants must delete the parenthetical information. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. **Claims 1, 12 and 37 are objected to** because Applicant's preamble must state the intended use or purpose of the invention, see 48 U.S.P.Q.2d (BNA) 1225, 1230-1231 (Fed Cir. 1998).

5. **Claims 23-29 are objected to** under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The parent claim 22 recites a method and claims 23-29 are further limiting a product instead of the method.

6. **Claims 29 and 36 are objected to** because of the following informalities:

7. Applicants use an alternative form of claiming that requires replacing the "or" in line 4 with –and-- for proper format.

8. At line 4 the Applicants must delete the choice of "a propagated signal". Under the USPTO Interim Guidelines for 35 U.S.C. 101, carrier waves (i.e. propagated signals) are not considered patentable.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. **Claims 22-29 are rejected** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. **Pursuant to claim 22**, Applicants recite a method of making a computer readable medium, however the claimed steps of the method lack any method steps to achieve the method's purpose. Encoding a circuit design on a computer readable medium product does not *make or manufacture* a computer readable medium product. Further, it is unclear how Applicants make a computer readable medium product.

12. **Claim 22-29 are rejected** under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention.

13. Applicant's invention is directed toward encoding or storing a circuit design method on computer readable media for subsequent execution or use. Applicant's invention does not make, manufacture or otherwise construct computer readable media.

14. For examination purposes, examiner treats claim 22 as reciting --A computer readable medium product comprising an executable method for analyzing a circuit design or model, the method comprising:--.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of claims 1, 2, 6, 7, 22, 23, 28, 29, 37, 38, 41 and 42

16. Claims 1, 2, 6, 7, 22, 23, 28, 29, 37, 38, 41 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spencer et al. (Spencer) (US Patent 6,405,352).

17. Spencer discloses a method of designing, analyzing and comparing timing models.

18. Spencer lacks a correction factor based on a variation between timing responses; however, Spencer does disclose the use of delta models (Spencer, Col. 5, ll. 45-46, Fig. 5 #504). It would have been obvious to one of ordinary skill in the art that delta models are analogous to a correction factor, because they are based on a variation or comparison between timing responses of two circuit models, and accordingly function as correction factors in a timing analysis (Col. 5, ll. 48-51).

19. **Pursuant to claims 1, 22 and 37**, Spencer discloses a method (Spencer, Col. 1, ll. 45-48), a computer readable medium product (Spencer, Col. 5, ll. 58-59) and a system (Spencer, Col. 2, ll. 15-16) for performing the method, the method comprising:

(a) obtaining a first estimated timing response (Spencer, Fig. 4 #410) of a first circuit path (Spencer, Col. 3, ll. 23-24) using a first timing model (Spencer, Col. 4, ll. 29-30, Col. 5, ll. 32-34, base chip model);

(b) obtaining a second estimated timing response (Spencer, Fig. 5 #508) of the first circuit path using a second timing model (Spencer, Col. 5, ll. 48-51, delta model);

(c) generating a circuit design using the corrected timing response (Spencer, Col. 2, ll. 47-50, Col. 5, ll. 48-53);

(d) encoding the circuit design onto the computer readable medium product (Spencer, Col. 5, ll. 58-59).

(e) applying the results of the delta model (Col. 5, ll. 48-51) to the timing model.

20. **Pursuant to claims 2, 23 and 38**, Spencer discloses obtaining estimated timing responses, wherein RC Delays and net capacitance values are used to generate timing runs for analysis, of a plurality of circuit paths using the first timing model (Spencer, Col. 5, ll. 31-32).

21. **Pursuant to claims 6, 28 and 41**, Spencer discloses wherein generating a correction factor (delta model) includes comparing the first estimated timing response and the second estimated timing response (Spencer, Col. 5, ll. 45-46).

22. **Pursuant to claim 7 and 42**, Spencer discloses wherein applying the correction factor includes adjusting the first estimated timing response based on the correction factor (Fig. 5 #'s 506, 508, wherein the model is timed using RC delays and net capacitance from the delta model).

23. **Pursuant to claim 29**, Spencer discloses wherein the computer readable medium product is selected from a group consisting of a random access memory, a read only memory, a magnetic tape, a magnetically encodable disk, an optically encodable tape, or an optically encodable disk (Spencer, Col. 5, ll. 60-65).

Rejection of claims 3-5, 8, 9, 24-27, 39 and 40

24. Claims 3-5, 8, 9, 24-27, 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spencer et al. (Spencer) (US Patent 6,405,352) in view of Kidd et al. (Kidd) (US Patent 6,834,379).

25. Spencer teaches the limitations of the claims from which claims 3-5, 8, 9, 24-27, 39 and 40 depend.

26. Spencer does not explicitly disclose selecting the first circuit path from the plurality of circuit paths.

27. Kidd does disclose selecting the first circuit path (Kidd, Fig. 8 #72) from the plurality of circuit paths (Kidd, Fig. 8 #70),

28. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify Spencer with Kidd in order to apply the correction factor to the selected paths of the first timing model, wherein the estimated timing responses of the plurality of circuit paths could be adjusted based on the correction factor (Spencer, Fig. #508, Delta Model). Modifying the invention of Spencer with Kidd would improve efficiency in the design process so that a chip manufacturer or designer can converge on a timing objective for a chip design more quickly (Spencer, Col. 2, ll. 49-

50), thus improving a way of modeling the timing of complex circuits (Applicant, Page 1, Paragraph 4).

29. **Pursuant to claim 3, 24, 25 and 39**, Spencer in view of Kidd discloses adjusting the estimated timing response based on the correction factor (Spencer, Col. 5, ll. 48-51, Fig. 5, #508, delta model).

30. **Pursuant to claims 4, 26 and 40**, Spencer in view of Kidd discloses a netlist used in describing the plurality of circuit paths, wherein Spencer discloses net names and net attributes (Spencer, Col. 3, ll. 27-28) and Kidd discloses the synthesis of a Resistor Transistor Logic (RTL) description to a netlist (Kidd, Col. 1, ll. 43-45, Fig. 1 #12).

31. **Pursuant to claim 5 and 27**, Spencer in view of Kidd discloses wherein obtaining a second estimated timing response includes providing the netlist to a modeling tool employing the second timing model. (Spencer, Col. 5, ll. 3-6) (Kidd, Col. 1, ll. 56-58).

32. **Pursuant to claims 8 and 9**, Spencer does not explicitly disclose including an estimated signal propagation delay and an estimated signal propagation time.

33. Kidd does disclose wherein the first estimated timing response (Kidd, Col. 3, ll. 45-49, Abstract Model) includes (as per claim 8) an estimated signal propagation delay (worst case delay) and (as per claim 9) an estimated signal propagation time (Kidd, Col. 1, ll. 67, Col. 2, ll. 1-2).

34. It would have been obvious to one of ordinary skill in the art to modify Spencer with Kidd in order to predict and verify timing paths and converge on a timing objective

for a chip design more quickly, improving the speed of circuit path timing predictions (Applicant, Page 1, Paragraph 1) (Kidd, Col. 1, ll. 10-16) (Spencer, Col. 2, ll. 49-50).

Rejection of claims 12-15, 18, 19, 30-33 and 36

35. Claims 12-15, 18, 19, 30-33 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Spencer et al. (Spencer) (US Patent 6,405,352) in view of Kidd et al. (Kidd) (US Patent 6,834,379).

36. Spencer discloses a method of designing, analyzing and comparing timing models.

37. Spencer lacks a correction factor based on a variation between timing responses; however, Spencer does disclose the use of delta models (Spencer, Col. 5, ll. 45-46, Fig. 5 #504).

38. It would have been obvious to one of ordinary skill in the art that delta models are analogous to a correction factor, because they are based on a variation or comparison between timing responses of two circuit models, and accordingly function as correction factors in a timing analysis (Col. 5, ll. 48-51).

39. Spencer further does not explicitly disclose the use of coarse and refined estimated timing responses with the two circuit models, wherein the timing models for said timing responses have associated accuracies.

40. Kidd does disclose abstract and debug models, wherein the debug models have accuracies that are more refined and detailed than the abstract models.

41. It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify Spencer with Kidd in order to predict and verify timing

paths and converge on a timing objective for a chip design more quickly, improving the speed of circuit path timing predictions based on differences in the models (Applicant, Page 1, Paragraph 1) (Kidd, Col. 1, ll. 10-16) (Spencer, Col. 2, ll. 49-50).

42. **Pursuant to claims 12 and 30**, Spencer in view of Kidd discloses a method of designing, analyzing and comparing timing models, and a computer readable medium product (Spencer, Col. 5, ll. 58-59) for performing the method, the method comprising:

(a) obtaining coarse estimated timing responses (Kidd, Col. 3, ll. 54-56) for a plurality of circuit paths (Kidd, Col. 3, ll. 7-9, timing paths) using a first timing model, the first timing model (Kidd, Col. 3, ll. 6-9, abstract model) having a first accuracy (Kidd, Col. 3, ll. 9-12);

(b) obtaining refined estimated timing responses (Kidd, Col. 4, ll. 25-35) for one or more selected circuit paths of the plurality of circuit paths using a second timing model having a second accuracy (Kidd, Col. 4, ll. 25, debug model) greater than the first accuracy (Kidd, Col. 4, ll. 31-32);

(c) generating a circuit design using the corrected timing response (Spencer, Col. 2, ll. 47-50, Col. 5, ll. 48-53);

(d) applying the results of the delta model (Spencer, Col. 5, ll. 48-51) to the timing model.

43. **Pursuant to claim 13 and 31**, Spencer in view of Kidd discloses the method wherein obtaining the coarse estimated timing responses includes estimating timing responses for the plurality of circuit paths using a modeling tool employing coarse timing

assumptions (Kidd, Col. 3, ll. 41-49, timing analysis tool, wherein worst case delay is retained and other paths are abstracted out).

44. **Pursuant to claim 14 and 32**, Spencer in view of Kidd discloses the method wherein obtaining refined estimated timing responses includes using a modeling tool employing refined timing assumptions (Kidd, Col. 3, ll. 41-42, Col. 4, ll. 25-27, wherein the debug model maintains detailed timing path info).

45. **Pursuant to claim 15 and 33**, Spencer in view of Kidd discloses a netlist used in describing the plurality of circuit paths, wherein Spencer discloses net names and net attributes (Spencer, Col. 3, ll. 27-28) and Kidd discloses the synthesis of a Resistor Transistor Logic (RTL) description to a netlist (Kidd, Col. 1, ll. 43-45, Fig. 1 #12).

46. **Pursuant to claims 18 and 19**, Spencer in view of Kidd does disclose wherein the first estimated timing response (Kidd, Col. 3, ll. 45-49, Abstract Model) includes an estimated signal propagation delay (worst case delay) and an estimated signal propagation time (Kidd, Col. 1, ll. 67, Col. 2, ll. 1-2).

47. **Pursuant to claim 36**, Spencer in view of Kidd discloses wherein the computer readable medium is selected from a group consisting of a random access memory, a read only memory, and a magnetically encodable disk (Spencer, Col. 5, ll. 63-65). Spencer in view of Kidd does not explicitly disclose a magnetic tape, an optically encodable tape or an optically encodable disk, however Spencer in view of Kidd does disclose that the invention applies equally regardless of the particular type of signal bearing media actually used to carry out the distribution (Spencer, Col. 60-63).

Allowable Subject Matter

48. **Claims 10, 11, 16, 17, 20, 21, 34 and 35** contain allowable subject matter.

49. **Claims 10, 11, 16, 17, 20, 21, 34 and 35** objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

50. The following is a statement of reasons for the indication of allowable subject matter:

51. **Pursuant to claims 10 and 20**, in a method of designing, analyzing and comparing timing models, the prior art does not fairly teach or suggest wherein the correction factor includes a scaling factor.

52. **Pursuant to claims 11 and 21**, in a method of designing, analyzing and comparing timing models, the prior art does not fairly teach or suggest wherein the correction factor includes an offset.

53. **Pursuant to claims 16 and 34**, in a method of designing, analyzing and comparing timing models, and a computer readable medium product for performing the method, the prior art does not fairly teach or suggest wherein generating a correction factor includes determining a statistical variation between the course estimated timing response of the one or more selected circuit paths and the refined timing estimates of the one or more selected circuit paths in the generation of a correction factor.

54. **Pursuant to claims 17 and 35**, in a method of designing, analyzing and comparing timing models, and a computer readable medium product for performing the method, the prior art does not fairly teach or suggest generating a correction factor for each of the plurality of circuit paths, wherein the statistical variation is equal to a

standard deviation of the correction factors for the plurality of circuit paths divided by mean of the correction factors for the plurality of circuit paths; and adjusting the coarse estimated timing responses of each of the plurality of circuit paths individually, if the statistical variation exceeds about twenty percent.

Conclusion

55. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick Sandoval whose telephone number is 571-272-7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through Friday.

56. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

57. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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